Effective IDDQ Testing method to identify the fault in Low-Voltage CMOS Circuits

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***Abstract*—A novel voltage delta IDDQ test method is presented for circuits working in low voltages. The proposed method can eliminate the any contribution from leakage due to the usage of differential IDDQ test method. The proposed method is successfully implemented on 1-bit, 32-bit and 100-adders circuits on IBM 130 nm technology and can detect faulty circuit only if short is activated from the applied logic input. Defining two voltage levels are critical for testing and will depend on the circuit under test.**

Keywords—IDDQ testing;Low voltage testing; voltage delta IDDQ

I. INTRODUCTION

IDDQ testing is a testing method for integrated circuit(IC) based upon measurement of steady state power-supply current. In steady state, when all switching transients are settled-down, a CMOS circuit dissipates almost zero static current (Leakage current ≈ on the order of few Nano amperes).However, in case of a defect such as gate-oxide short or short between two metal lines, a conduction path from power-supply (VDD) to ground (GND) is formed and subsequently the circuit dissipates significantly high current. This faulty current is a few orders of magnitude higher than the fault-free leakage current. Therefore monitoring this leakage current can distinguish the faulty IC with faulty free IC[1].

Although, the traditional IDDQ testing approach has worked for earlier technologies, it is not suitable for deep submicron technologies. As transistor geometries are reduced in new and emerging technologies, leakage current levels are rising with each technology node thus results a large variation in fault-free IDDQ. As fault free and faulty IDDQ distributions overlap, it becomes difficult to discriminate faulty chips. This will results in false rejects (yield loss) or false accepts (test escapes). Therefore, understanding whether these chips are defective or fault-free is important to minimize yield loss. It is important to define effective IDDQ testing strategy for the sub-threshold CMOS circuits in deep submicron circuits[1].

Several techniques have been proposed to make IDDQ testing feasible in deep submicron CMOS technologies. These can be characterized in to two main categories and those that target background current reduction during IDDQ testing and those that try to increase the immunity of IDDQ testing to background current fluctuation[2]. In first category, [3]proposed a method to increase the threshold value of the transistor by substrate bias during the testing period. However, applying different substrate bias during testing period will require special techniques and will be expensive. In [4]the use of dual-threshold and vector control techniques for the transistors in critical paths are discussed. The application of IDDQ testing at lower temperatures is reported in [5]. It was proposed to measure the IDDQ current at two different temperatures (T1 and T2) where T2<T1. The difference for defective chips is significantly less than for defect free chips because of defect-induced extra leakage current. The higher cost is the main limitation of this method. Anton et al [6] presents a test technique that employ two different supply voltages(2 V and 3.8 V) for the same IDDQ pattern. The results of the two measurements are subtracted in order to eliminate the inherent sub threshold leakage. The IDDQ threshold is defined based on the ΔIDDQ value. In the second category, the ΔIDDQ testing technique is introduced to increase IDDQ testing quality[7]. According to this method, differences (delta) in IDDQ measurements for consecutive test vectors for a chip are obtained. In a fault free chip the mean delta is expected to be small while defective chip has much higher value[7].

The proposed method in this paper is based on differential IDDQ testing over voltage. The main difference of the proposed method and method in[6] is that the proposed method is applied on a circuit working in ultra-low voltages and usage of statistical distribution to identify the faulty chips instead of the single threshold value. The method is very similar to the differential IDDQ testing over temperature. Instead of using a different temperature value this method uses different voltage values to differentiate the faulty circuits with fault free circuit.

II. PROPOSED METHODOLOGY AND EXPECTED OUTCOME

The proposed method is based on voltage delta IDDQ testing and on following assumptions. Intragate shorts which happen within a CMOS gates are considered as a fault model in the proposed method. The fault is modeled with a fixed resistance. Inputs are set to logic 1 (A=B=Cin=1) during all simulation for simplicity. Number of iterations on Monte Carlo is set to 400 to save duration of the simulation. The proposed voltage delta IDDQ testing method consist of following steps.

1) Introduce three random faults to three locations one at a time for 1-bit adder
2) Run VDD sweep and calculate deltaIDDQ to identify the two suitable voltage levels and the fault resistance value to run voltage delta IDDQ testing.(V1,V2 and fault resistance) (DeltaIDDQ= IDDQ(Faulty)-IDDQ(Faultfree))

3) Generate IDDQ distribution for each fault for 1-bit adder as follows

a) Generate IDDQ distribution at V1 for fault free and faulty circuit

b) Generate IDDQ distribution at V2 for fault free and faulty circuit

4) Repeat the procedure a and b for 32-bit adder (1-bit has 1 fault at location 1 and 31-bits are fault free).

5) Repeat the procedure a and b for 100-bit adder (1-bit has 1 fault at location 1 and 99-bits are fault free).

The Figure 1 represents the expected wave form of the step 3 to 5.If ΔIDDQFaulty>>ΔIDDQFaultFree, the chip can be considered as a defective circuit. The proposed method will increase the non-overlapping region between IDDQ distribution of faulty free chip and faulty chip at V2 so that there will be no false rejects or false accepts.

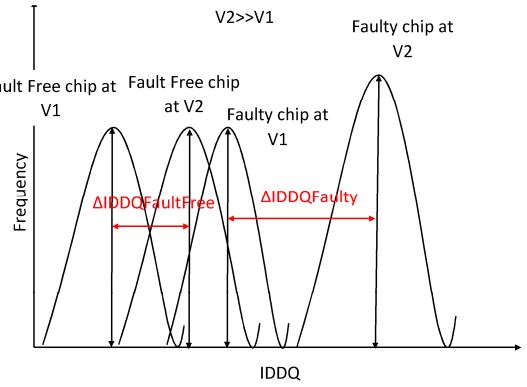

Figure 1.Expected IDDQ distribution of the faulty and fault free chip at two different voltages

The 1-bit adder circuit with faults location is shown in Figure 2.

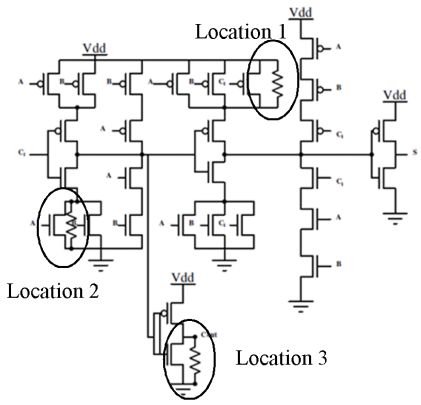

Figure 2. The 1-bit adder circuit with faults location

The DeltaIDDQ for 1-bit adder with a fault at location 1 with different input voltages is shown in Figure 3.If the fault resistance value is in between 0 Ω - 1000Ω, V1 and V2 voltage can be chosen as 0.1 V and 0.5 V to have a higher DeltaIDDQ. The maximum metal sheet resistance is 0.0709 Ω/squre for IBM 130 nm technology[8] and therefore assumption of metal short resistance is in between 0 and 1000Ω will be a valid assumption for the proposed method. The fault resistance is set to 100 Ω during the simulation.

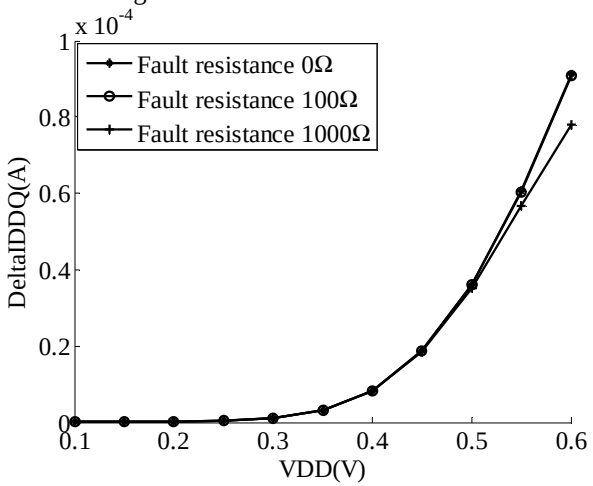

Figure 3.DeltaIDDQ vs VDD for 1-bit adder with different fault location values.

III. SIMULATION RESULTS

The proposed IDDQ test method is first verified using 1-bit adder in Cadence, with 130 nm IBM technology.

A. Voltage delta IDDQ testing on 1-bit adder

The IDDQ distribution for each fault for 1 bit adder is shown in Figure 4,Figure 5 and Figure 6.

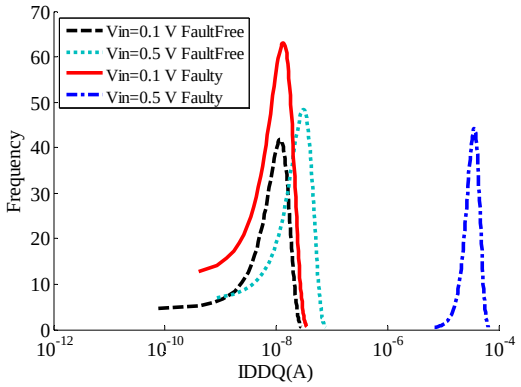

Figure 4. The IDDQ distribution for 1-bit adder when the fault is at location 1

According to Figure 4 and Figure 6 , it can be clearly seen that ΔIDDQFaulty>>ΔIDDQFaultFree. Therefore, faults at location 1 and 3 can be detected using the proposed method. On the other hand fault at location 2 cannot be identified for this circuit. This is because fault at location 2 will not create any direct path between VDD and GND based on applied logic input and hence there will be no extra current going through that path. A metal short can be detected only when two requirements are met simultaneously. The two requirements are activating a direct conducting path from VDD to the GND and satisfying the IDDQ test limit[4].Therefore, when A=B=Cin=1,the fault at location 2 cannot be detected using the proposed method. It can be seen that for larger circuits, faulty and faulty free IDDQ

distribution have an overlap at V1. This is because faulty current will be the same as faulty free current at lower voltage.

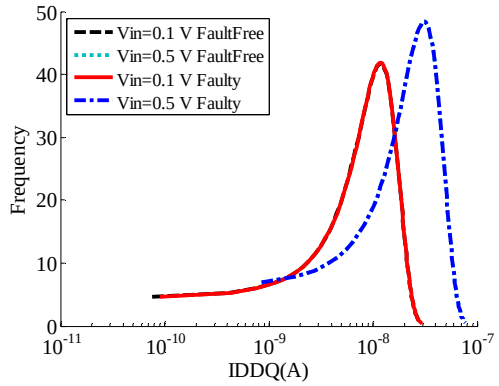

Figure 5. The IDDQ distribution for 1-bit adder when the fault is at location 2

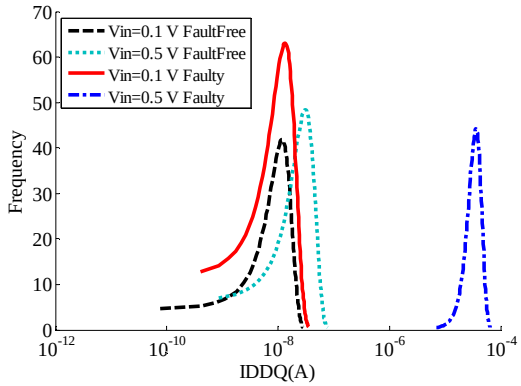

Figure 6. The IDDQ distribution for 1-bit adder when the fault is at location 3

B. *Voltage delta IDDQ testing on 32-bit adder*

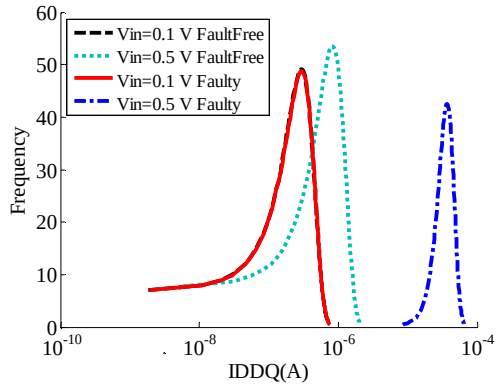

Figure 7. The IDDQ distribution for 32-bit adder when the fault is at location 1 at 0^{th} bit

It is also noted that at 0.5 V, the faulty IDDQ distribution is getting closer to the fault free IDDQ distribution for larger circuit. This result is expected for 32 and 100 bit adders since introduction of single fault with one block while all other blocks are fault free which is the worst case scenario for the proposed method. Therefore, deciding of V2 is critical for the proposed method and it depend on the circuit under test and total fault resistance value. For lager circuits difference between V1 and V2 will be higher compare to small circuit blocks.

C. *Voltage delta IDDQ testing on 100-bit adder*

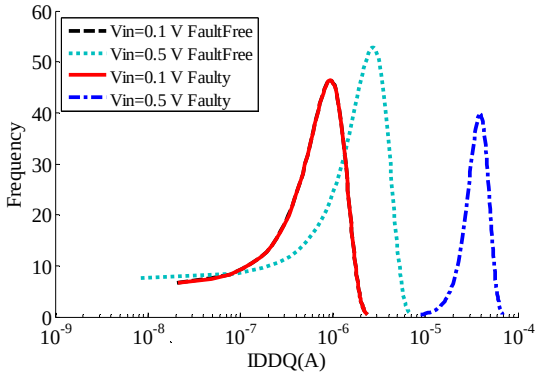

Figure 8. The IDDQ distribution for 100-bit adder when the fault is at location 1 at 0^{th} bit

IV. CONCLUSION

A novel voltage delta IDDQ test method is presented for circuits working in low voltages. The method can successfully differentiate faulty circuit if the fault resistance (range from 0Ω to 1000Ω) activated with applied logic input. Defining two voltage levels are critical for the method and it is depended on the circuit under test. The method can eliminate the leakage current contribution which is a critical factor for deep submicron devices due to the usage of differential IDDQ test method to define a threshold for the faulty circuit.

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